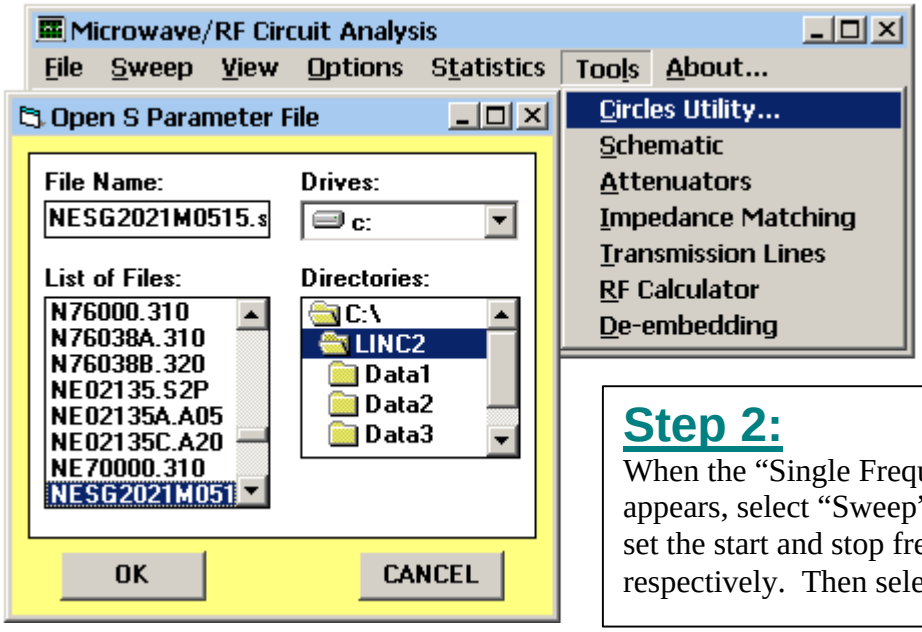
Designing an LNA with Improved Input Match

This procedure will show how to design a low noise amplifier (LNA), for a given noise figure, while at the same time applying the best (return loss) match to both ports. When the input matching circuit, M1, transforms the system impedance to Γopt (for minimum noise), or some other point on a given noise circle, the input RL (return loss) becomes a function of the load reflection coefficient (Γ_L). If the output matching circuit, M2, terminates the device with a conjugate match ($\Gamma_L = \Gamma out^*$) then a certain input RL will result. However, the output can be mismatched in such a way as to improve the input RL without changing the input circuit (keeping the source impedance set for a given noise figure).

The LINC2 Circles Utility will be used to find a tradeoff between input and output RL so that both will be equally optimum. The input match (transformed source impedance) will be set for a given noise figure (NF=1.39 dB) and will not be changed in the process.

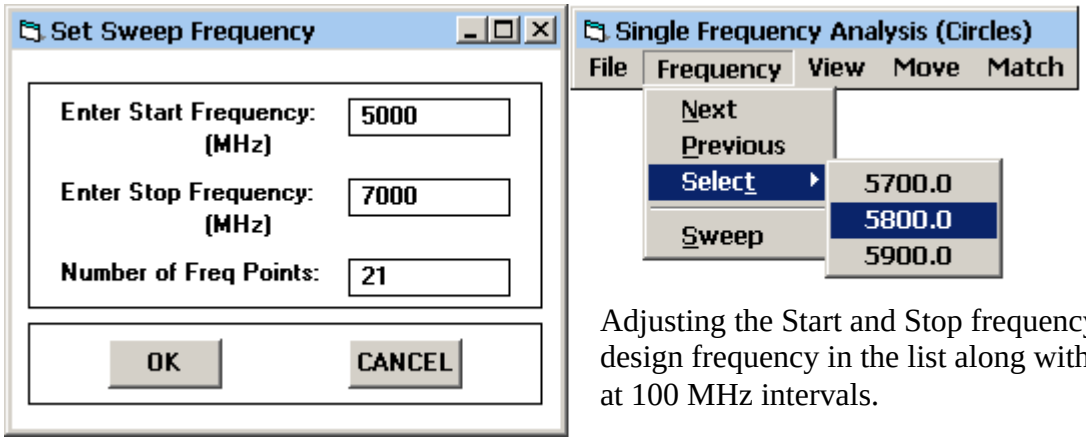


Step 1:

Launch the Circles Utility from the "Tools" menu and select the two-port S Parameter file for the transistor. For this example, use NESG2021M0515.S2P.

Step 2:

When the "Single Frequency Analysis (Circles)" window appears, select "Sweep" from the "Frequency" menu and set the start and stop frequencies to 5000 and 7000 MHz respectively. Then select 5800 (MHz) from the menu list.

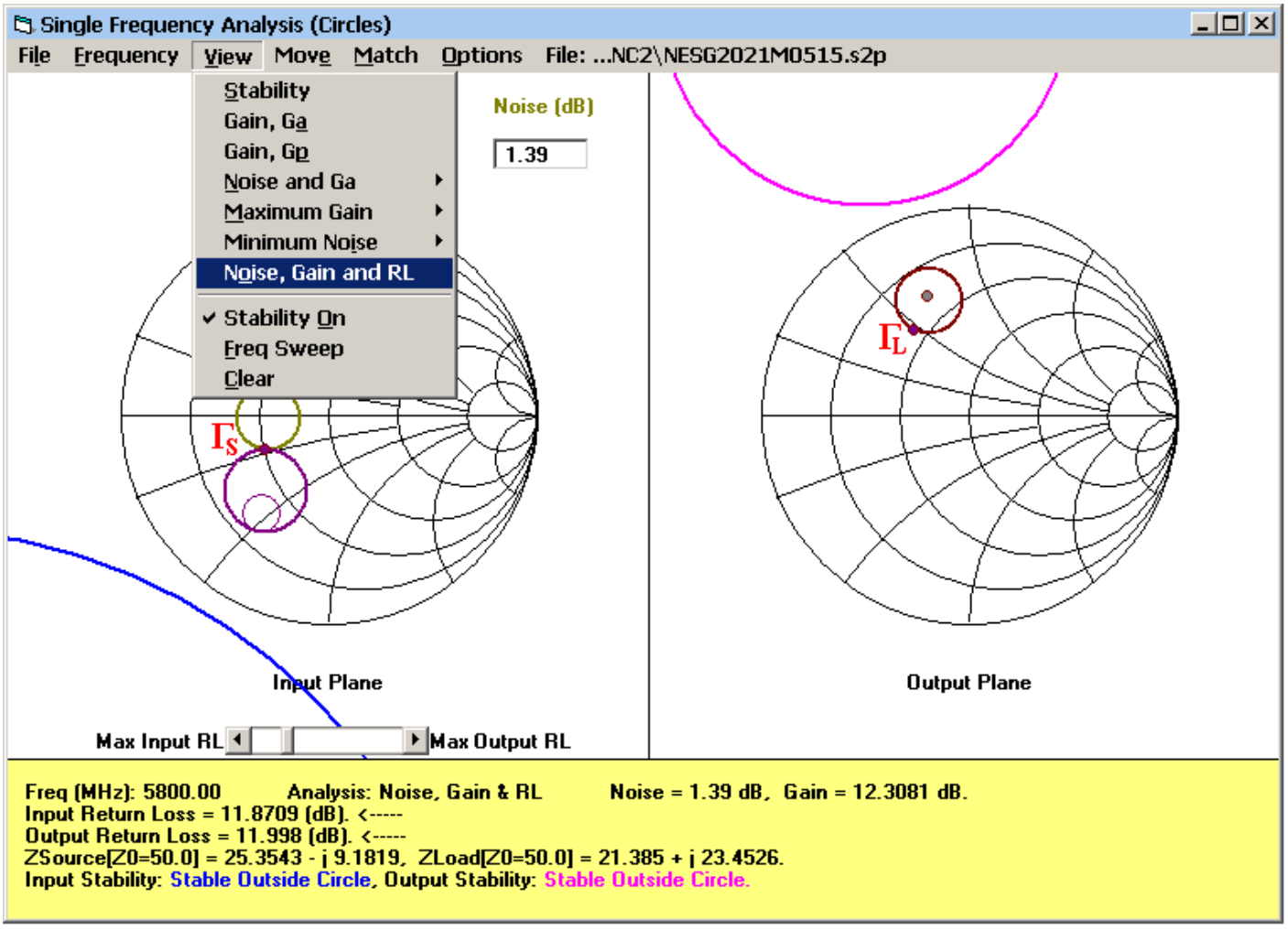


Adjusting the Start and Stop frequency as shown includes the design frequency in the list along with 20 other analysis points at 100 MHz intervals.

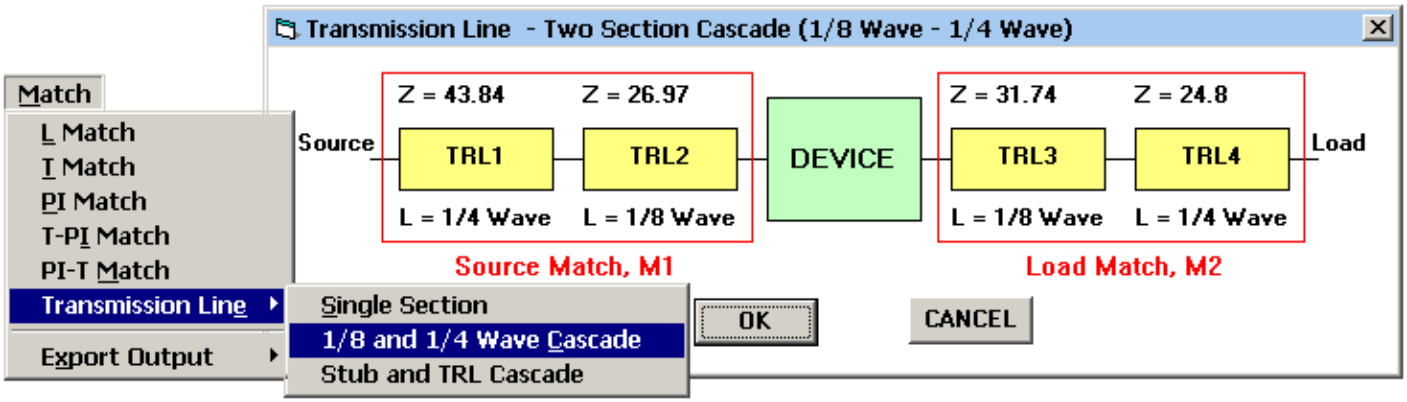
Step 3:

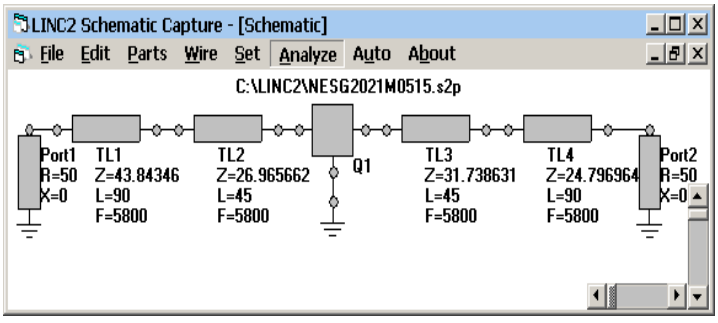
Select "Noise, Gain and RL" from the View menu. By default the source reflection coefficient is set to Γopt for minimum noise (1.33 dB). Change the value to 1.39 in the noise input box. Then press ENTER to plot the 1.39 dB noise circle. Move the slider control to the left (toward Max Input RL) until the input and output return losses are approx. equal at nearly 12 dB (or press ENTER and enter 12 dB directly).

The 12 dB (RL) mismatch circle is plotted on the output plane. Near the center of this circle is the conjugate output match point. However, the chosen Γ_L is a point on the circle such that the input RL is also nearly 12 dB and Γs is the intersection point of the 11.87 dB (RL) input mismatch and noise circle.



Step 4: Select "Transmission Line > 1/8 and 1/4 Wave Cascade" from the "Match" menu.





Step 5 (run the simulation):

Click "OK" to accept the matching topology (shown above). The schematic (left) will be automatically generated. Click "Analyze" and then "View>Plot" to see the results. The GRAPH reveals that a gain of 12.3 dB has been achieved at 5800 MHz. The associated noise figure will be about 1.39 dB. "View >Smith Chart" shows nearly 12 dB RL at each port.