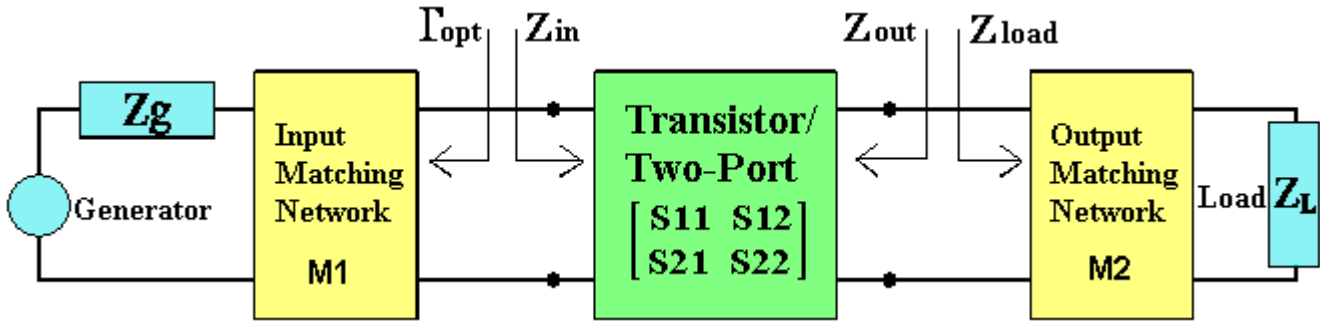
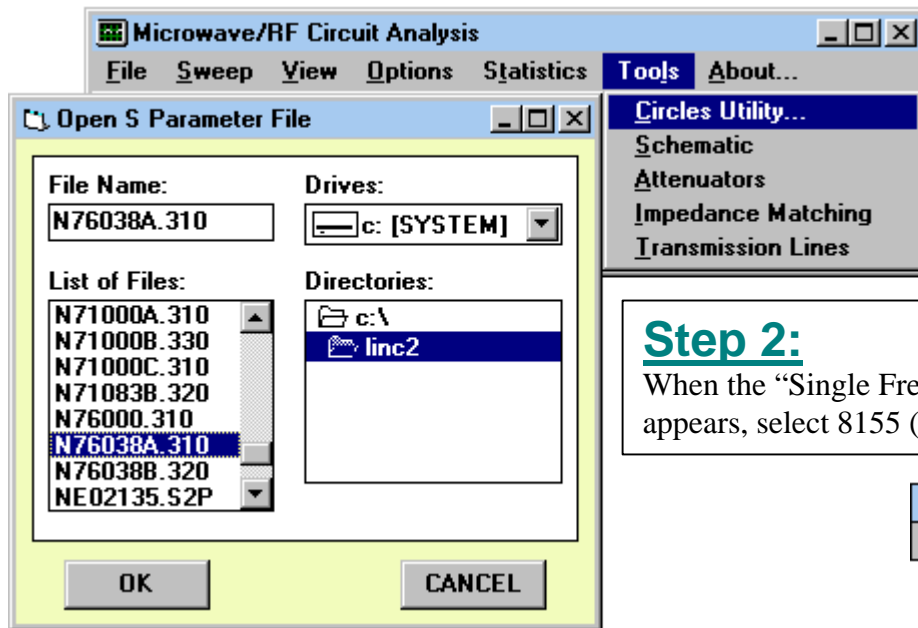


# Designing a Low Noise Amplifier (LNA)



The figure above shows a transistor (represented by its two-port S Parameters) connected to a source and load via input and output matching networks. In this example, input circuit M1 will present the optimum reflection coefficient,  $\Gamma_{opt}$ , at the input port for best noise performance. At the output port, matching circuit M2 will provide a conjugate match to the load termination. This will result in an amplifier with minimum noise figure. It should be noted that while a conjugate match exists at the output, the input port cannot (in general) be matched for gain and low noise simultaneously. LINC2 has the capability to improve the input match while maintaining minimum noise figure. However, for expediency in this example, we accept a higher input VSWR as the tradeoff for minimum noise.

The Circles Utility will be used to solve the matching problem for the general case, where the transistor is bilateral. In this case  $S_{12} \neq 0$ , and  $Z_{in}$  and  $Z_{out}$  are NOT simply equal to  $S_{11}$  and  $S_{22}$  respectively.

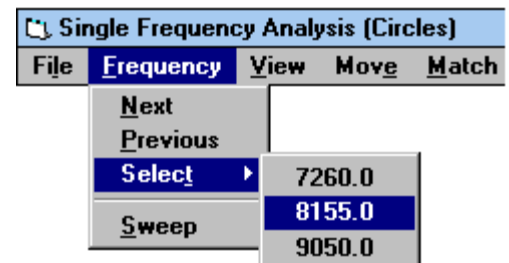


## Step 1:

Launch the Circles Utility from the "Tools" menu and select the two-port S Parameter file for the transistor. For this example, use N76038A.310.

## Step 2:

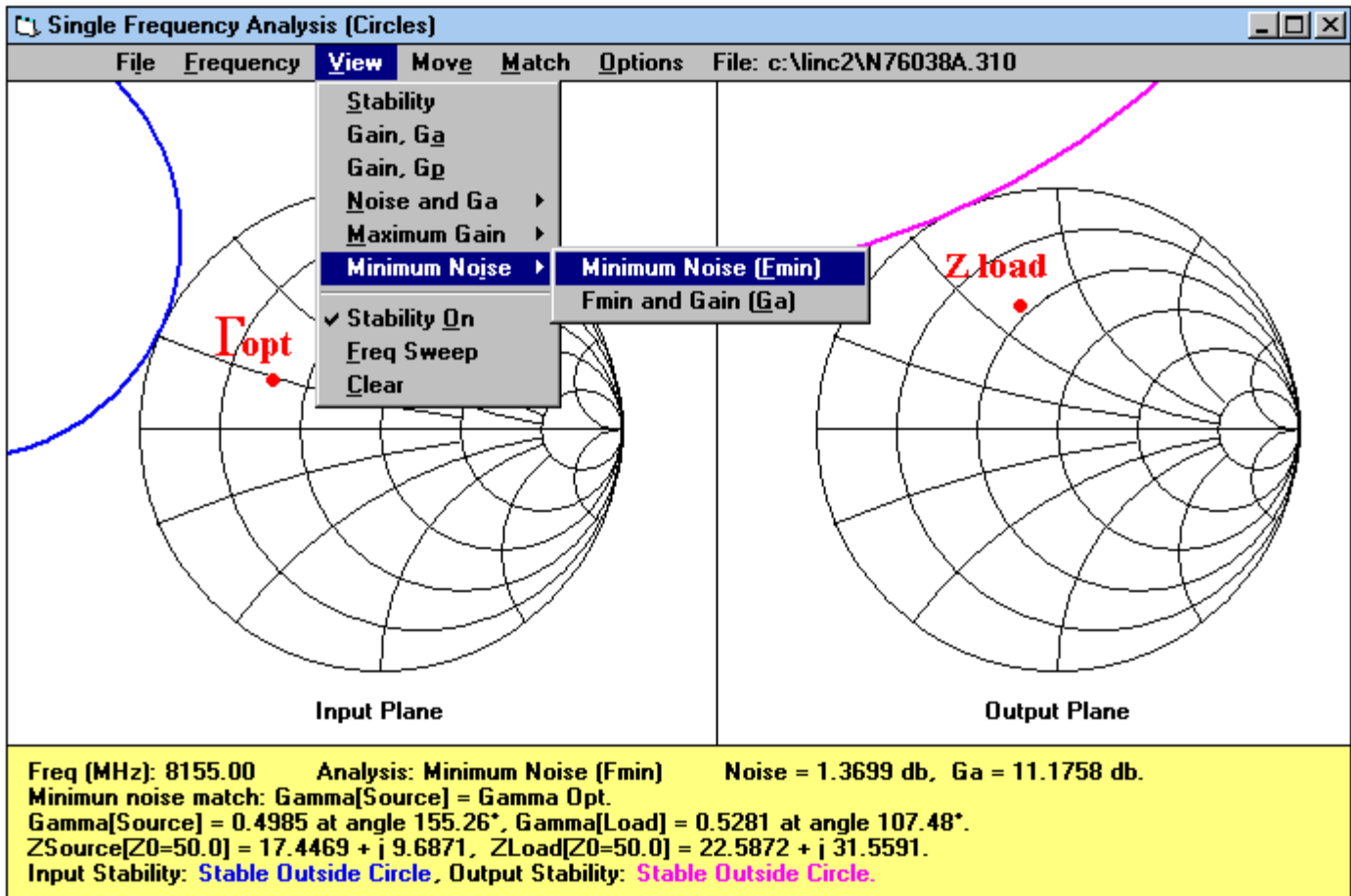
When the "Single Frequency Analysis (Circles)" window appears, select 8155 (MHz) from the "Frequency" menu.



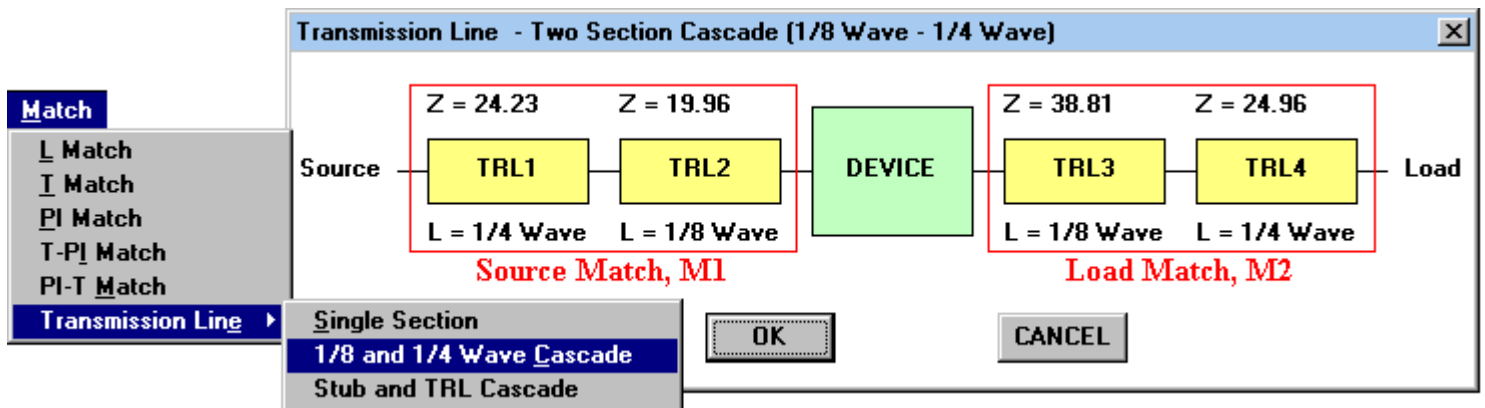
In step 2 the available frequencies can be changed by editing the "Sweep" dialog box from the "Frequency" menu.

## Step 3:

Select "Minimum Noise > Minimum Noise (Fmin)" from the "View" menu. A single point (red dot) appears in each of the input and output Smith Chart views. In the input plane, the point called  $\Gamma_{opt}$  represents the impedance the transistor must see looking toward the source. In the output plane, the point called  $Z_{load}$  represents the impedance the transistor must see looking toward the load. This is shown in the following figure (next page). →



**Step 4:** Select “Transmission Line > 1/8 and 1/4 Wave Cascade” from the “Match” menu.



### Step 5 (run simulation):

Click “OK” to accept the matching topology (shown above). The circuit schematic will be generated automatically and placed in the schematic window (right). Click “Analyze” and then “View>Plot” to see the results. The GRAPH reveals that a gain of 11.175 dB has been achieved at 8155 MHz. The associated noise figure will be about 1.37 dB.

