

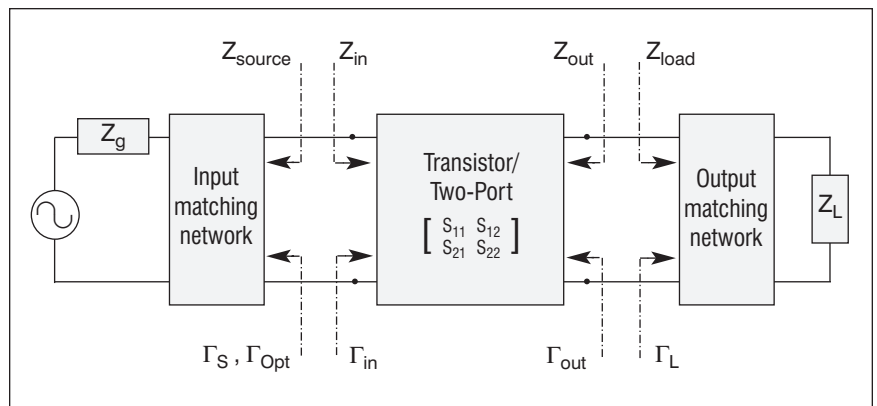
LNA Design Uses Series Feedback to Achieve Simultaneous Low Input VSWR and Low Noise

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The noise figure of a single stage transistor amplifier is a function of the impedance applied to the input terminals of the transistor. This impedance, called the source impedance, is shown in Figure 1 as Z_{source} . Typically the source impedance that produces a conjugate match to the input impedance of the transistor (Z_{in}) is not the same impedance as would be required to produce a minimum noise figure for the amplifier. Therefore, the problem exists that the input matching network can be tuned for low VSWR (conjugate match) or low noise figure but not both simultaneously. This article describes a feedback technique for simultaneously achieving low input VSWR and low noise figure in LNAs employing Field Effect Transistors (FETs). It will be shown that in-band stability is also improved as an additional benefit of the negative feedback employed.

Although the technique presented here can be applied over a wide range of RF and microwave frequencies, all numerical results presented will be for an LNA designed for operation in the PCS cellular band at 1.9 GHz.

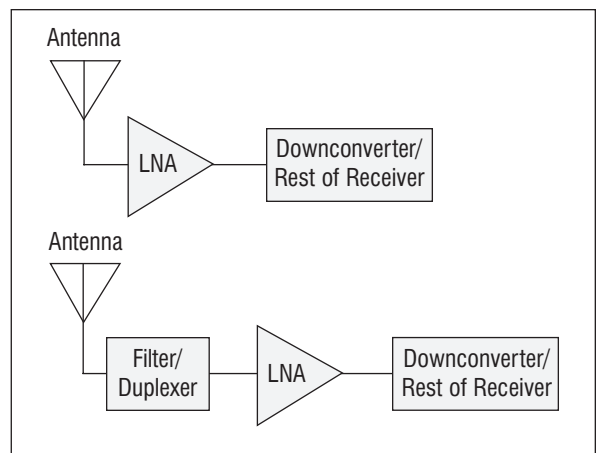
As shown in Figure 2, the importance of LNA input matching depends on the application. In a receive only system, such as a satellite receiver, the LNA might be connected directly to an antenna. The LNA input match is typically designed to achieve minimum input noise figure, accepting a relatively large input mismatch.



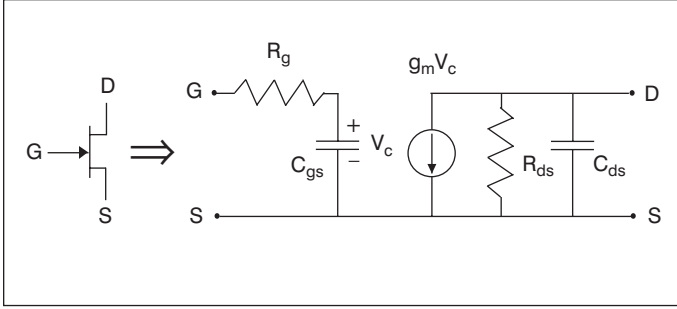
■ Figure 1. The generalized analytical form of the low noise amplifier.

The overall system performance is probably not substantially affected by the mismatch. This configuration is shown at the top of Figure 2.

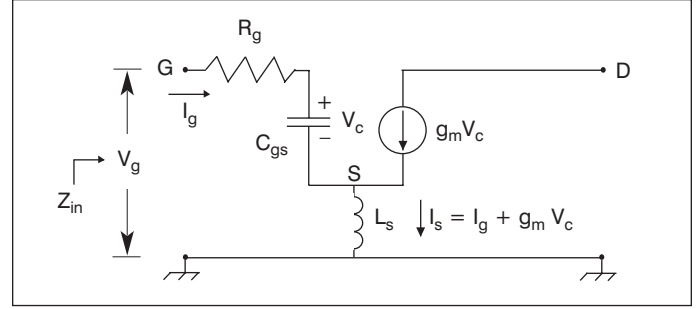
In many fully duplex systems the transmit-



■ Figure 2. Two LNA implementations. Top: System less sensitive to LNA input match. Bottom: System more sensitive to LNA input match.



■ Figure 3. FET symbol (left) and simplified FET model (right).



■ Figure 4. FET model with external source inductance.

ting and receiving sections share a common antenna. In CDMA or AMPS cellular telephones, for example, a duplexer separates the receive and transmit bands at the antenna. In the configuration shown at the bottom of Figure 2, where a filter or duplexer precedes the LNA, the filter's performance can be degraded by the mismatch and system performance may suffer. In this situation it is desirable to design the input match for low VSWR as well as minimum noise.

The Input/Output Match

In the following analysis, the simplified unilateral MESFET model of Figure 3 will be used. In this model only the elements of first order importance have been retained [1, 2]. This will simplify the mathematics while preserving the effects that we wish to study.

The location on the Smith Chart labeled Γ_{opt} in Figure 5 is representative of the optimum source impedance (Z_{source}) required for minimum noise figure for a typical FET suitable for operation as an LNA at similar frequency and bias conditions as covered in this paper. Using a NEC 34018 FET operating at 1960 MHz with V_{ds} and I_{ds} biased at 2 volts and 20 mA respectively, the value of Γ_{opt} is 0.6168/41.36°. This FET and operating conditions will be used as an example throughout the rest of this article.

A transistor must have a conjugate match at both ports in order to achieve maximum gain and minimum VSWR. However, a conjugate match to Γ_{opt} requires $Z_{in} = \Gamma_{opt}^* = 0.6168/-41.36^\circ$. This equates to a $Z_{in} = 68.15 - j89.67$ Ohms. Typical values of C_{gs} are in the order of a few tenths of a pF [3]. This presents more capacitive reactance than needed. Additionally, R_g falls far short of the 68 ohms needed for a noise match. Typical values of R_g can be significantly less than 10 ohms [3]. What is needed, then, is a method by which the effective input resistance can be increased while at the same time decreasing the capacitive reactance. This must be accomplished without adding noise to the system. The next section describes a noiseless feedback technique that will accomplish this goal.

Series feedback technique

In 1928 H. Nyquist showed that the noise from any impedance is determined by its resistive component [4]. Consequently, if an ideal lossless element is used to pro-

vide the feedback then the minimum noise measure is unaffected [5]. Figure 4 adds an ideal inductor in series with the source lead of the FET in Figure 3. The additional inductance between the source and ground provides lossless negative series feedback to accomplish the following results.

The voltage developed across the internal C_{gs} capacitor is $V_c = I_g / (S C_{gs})$ where S is the complex frequency variable $S = \sigma + j\omega = j\omega$.

$$Z_{in} = V_g / I_g = (I_g R_g + V_c + I_s S L_s) / I_g$$

Substituting $I_g / (S C_{gs})$ for V_c and $(I_g + g_m V_c)$ for I_s gives:

$$Z_{in} = [I_g R_g + I_g / (S C_{gs}) + (I_g + g_m V_c) S L_s] / I_g$$

Again, substituting $I_g / (S C_{gs})$ for V_c and dividing through by I_g gives:

$$Z_{in} = R_g + 1 / (S C_{gs}) + S L_s + g_m [I_g / (S C_{gs})] S L_s / I_g$$

Rearranging and canceling out I_g in the last term yields the result:

$$Z_{in} = R_g + g_m L_s / C_{gs} + S [L_s + 1 / (S^2 C_{gs})]$$

Substituting $S = j\omega$ into the above gives the input impedance as a function of frequency:

$$Z_{in} = R_g + g_m L_s / C_{gs} + j[\omega L_s - 1 / (\omega C_{gs})] \quad (1)$$

This is the new composite FET input impedance.

Equation 1 can be rewritten for clarity as follows:

$$Z_{in} = R_g + R_a + j[X_{Ls} - X_{Cgs}]$$

where $[R_a = g_m L_s / C_{gs}]$ is effectively an "added" input resistance.

The input impedance of the FET without feedback can be written down by inspection (from Figure 3) as $Z_{in} = R_g - j X_{Cgs}$. Thus, equation 1 indicates that feedback adds $R_a + j X_{Ls}$ to the FET's input impedance.

From the above result, it is clear that a real (resistive) component equal to $g_m L_s / C_{gs}$ has been added to the input impedance as well as a positive reactive component. Both of these effects move Z_{in} closer to Γ_{opt}^* .

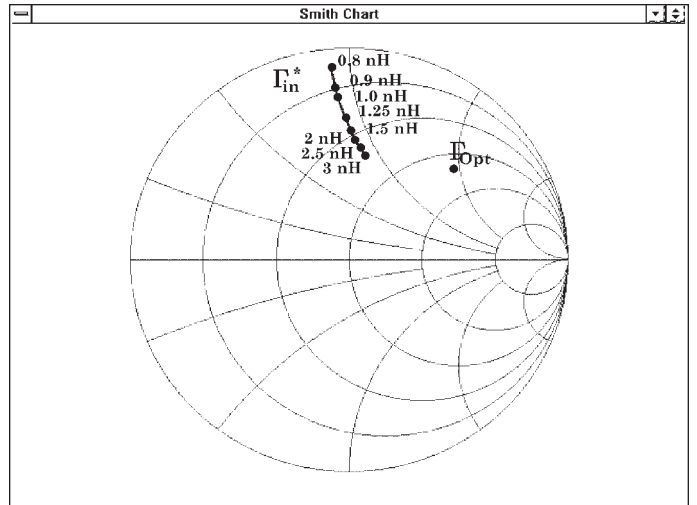
It can be shown that for the frequency and amount of feedback applied here that G_{opt} does not change appreciably. Hewlett-Packard has shown similar results with their low noise GaAs FETs, stating that “ Γ_{opt} remains relatively unchanged with the addition of source inductance” [6]. Thus, as Z_{in} moves closer to Γ_{opt}^* the distance between the noise match and the gain match on the Smith Chart decreases, facilitating a simultaneous gain and noise match.

Since the feedback is negative, there is an accompanying decrease in gain with increasing feedback. Therefore, a compromise is generally made between the amount of improvement in VSWR/noise figure and the gain reduction one is willing to take.

Results

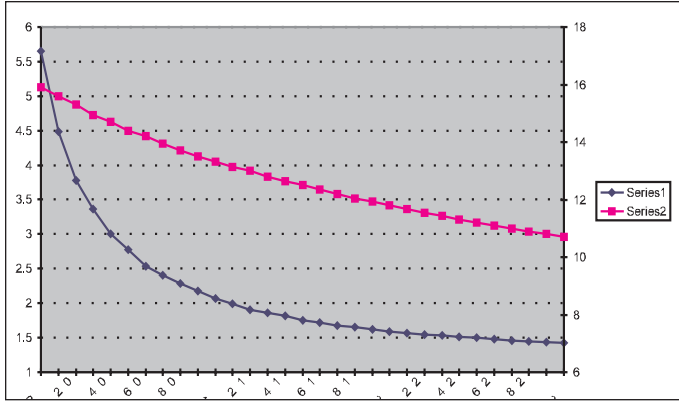
Figure 5 shows the results of increasing the source inductance from $L_s = 0.8$ nH to $L_s = 3$ nH. The plot indicates that Γ_{in}^* moved from $0.905/95.28^\circ$ to $0.4964/81.97^\circ$. This reduced the radial distance between Γ_{in}^* and Γ_{opt} from 0.736 to 0.402, a decrease of nearly 50 percent.

This plot was constructed with the aid of a simulation program (LINC2) developed by the author. The simulation was based on the FET's S-parameter data (including noise parameters for the device). The simulation was conducted with both ports (gate and drain) terminated



■ Figure 5. Source match vs. source lead inductance (L_s).

with their respective conjugate match impedances. The simulation started with $L_s = 0.8$ nH because smaller values of source inductance did not provide enough feedback to guarantee unconditional stability. Gain matching at both ports is not possible if the composite device is not unconditionally stable.



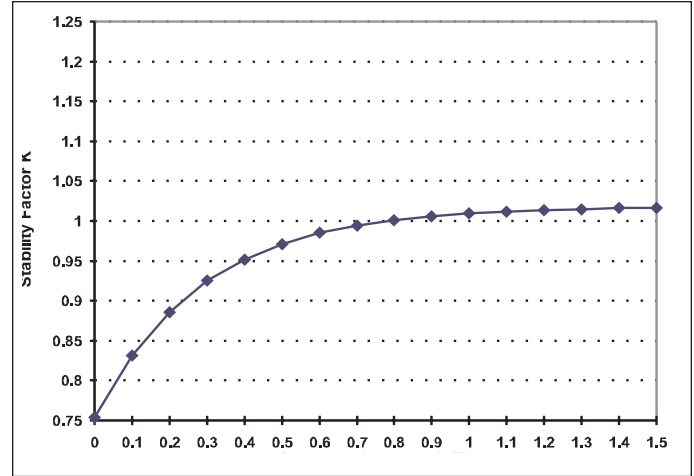
■ Figure 6. Input VSWR vs. source inductance.

The plot of Γ_{in}^* in Figure 5 moves along a contour of nearly constant reactance in a direction of increasing resistance. Equation 1 predicted the increasing resistive component ($g_m L_s / C_{gs}$). Since the capacitive reactance produced by C_{gs} is typically more than 10 times the reactance of L_s , it dominates the overall reactance. Therefore, equation 1 also predicted the arc of constant reactance in Figure 5 (C_{gs} is fixed and dominating).

Figure 6 shows that, for a minimum noise figure design, the input VSWR drops rapidly from 5.65 to 1.43 as the source lead inductance increases from 0 to 3 nH. Note the accompanying reduction in gain due to the effects of increasing negative feedback.

As Figure 7 indicates, the FET is potentially unstable without the addition of source inductance. As the source lead inductance is increased the stability factor increases rapidly. At $L_s > 0.8$ nH, $K > 1$ and the device is unconditionally stable.

However, it should be noted that for substantially larger values of L_s , the device becomes potentially unstable again. In addition, practical inductors have parasitic components that produce self resonance at higher frequencies. These parasitic resonances can cause instability above the operating frequency. Resistive termina-



■ Figure 7. Stability factor K vs. source inductance.

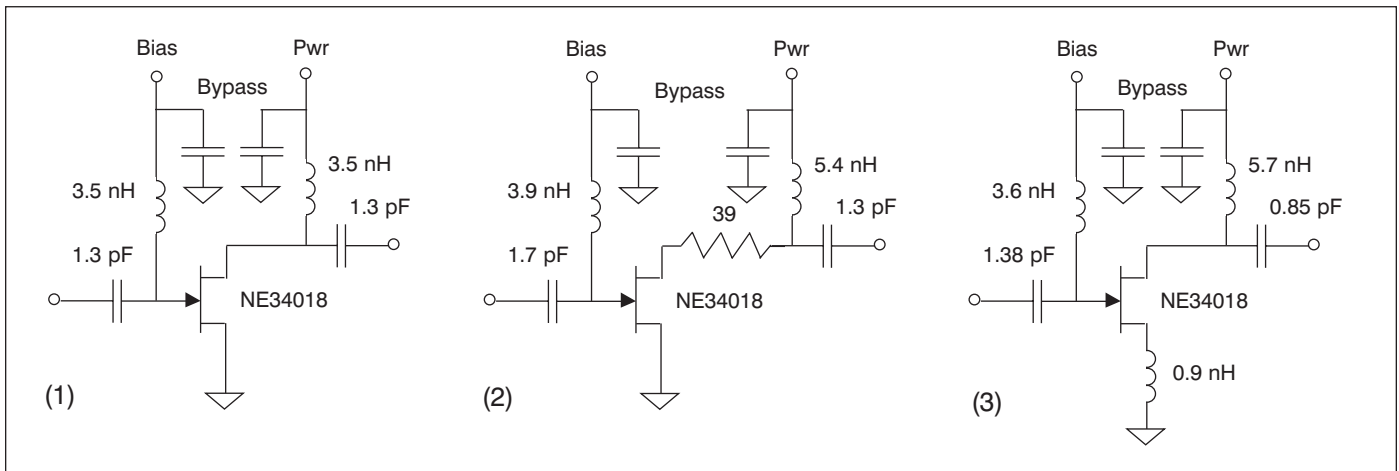
tions can be incorporated into the bias feeds in such a way as to enhance the stability above and below the operating frequency without appreciably affecting the input and output matching networks.

Figure 8 shows the results of three approaches to LNA design. In each case the common design goal was to maintain a noise figure of about 1 dB. In all three circuits the output port is matched.

In LNA circuit #1 the source is grounded and there was no attempt to stabilize the device. The gain is the highest of the three at 19 dB but the input VSWR is greater than 6:1. The amplifier is potentially unstable with $K = .75$.

In LNA circuit #2 the source is grounded and the drain is resistively loaded to achieve unconditional stability. The result is a substantial reduction in gain with an improved VSWR of 3:1.

In the third LNA circuit unconditional stability is achieved using a 0.9 nH source inductor without resistive loading. The result is a 1 dB additional reduction in gain while the input VSWR improved to better than



■ Figure 8. The three LNA configurations examined: (1) Grounded source (potentially unstable); (2) Grounded source, resistively stabilized; and (3) Source inductance for series feedback.

LNA Type NE34018@1.96 GHz/2 V/20 mA)	Gain (dB)	NF (dB)	Input VSWR	Output VSWR	Stability Factor K
1. Source grounded, no stabilization	19	1.1	6.16	1:1	0.754
2. Source grounded, stabilized by a 39 ohm series drain resistor	15.6	0.95	3.13	1:1	1.004
3. Stabilized by a 0.9 μ H source inductance, no resistor	14.6	0.95	1.43	1:1	1.006

■ **Table 1. Summary of the three approaches to LNA design.**

Frequency (MHz)	1930	1960	1990
Gain (dB)	14.94	14.94	14.47
NF (dB)	0.77	0.75	0.77
Input Return Loss (dB)	-18	-17.9	-17.8
Output Return Loss (dB)	-10	-10	-10
IIP ₃ (dBm)	+13.25	+13.25	+13.25
OIP ₃ (dBm)	+28.19	+28.19	+27.72

■ **Table 2. Measured performance of the NE34018 FET LNA, V_{ds} = 2 V, I_{ds} = 20 mA.**

1.5:1. Table 1 summarizes the three design approaches.

In these examples the output was terminated in its conjugate match. There exists a technique by which Z_{in}^* can be pushed further towards Γ_{opt} [7]. However, it generally requires that the output be mismatched. If the mismatch is large enough, a second amplifier may be needed to restore the output match.

Conclusions

Although only elements of first order importance were included in the FET model used for analysis, some useful predictions of FET noise matching were obtained. The simulation results were based on measured FET S-parameters and therefore serve to independently validate the analytical method used to arrive at equation (1) via the models of Figures 2 and 3.

Similar results were achieved in the lab where several prototype LNAs were built and tested. Table 2 shows performance measurements obtained from a prototype LNA using the same FET and operating conditions as in example 3 above.

Third order input and output intercept points, IIP₃ and OIP₃ respectively, are included in the measured performance data. They indicate that the amplifier's linearity is very good.

The prototype's input return loss exceeds the simulation results by at least 2 dB. This has been achieved at the expense of output return loss. The technique of trading output match for further improvements in input match was briefly mentioned above and is covered in ref. [7].

In conclusion, lossless feedback in the form of source inductance and a certain amount of output detuning can be effective methods of improving LNA input match while maintaining the noise figure near F_{min} (minimum noise figure).

Summary

This paper demonstrated through analysis and computer methods that a low noise match can be maintained while simultaneously matching for low VSWR in many FET LNAs. Specifically, series feedback in the form of a small amount of inductance introduced into the FET's source lead to ground made improvements to both the input match and in-band stability.

Some transistors yield more readily than others to the technique described here. A computer program was developed by the author and used to demonstrate how to quickly assess whether the addition of source inductance will yield positive results.

This technique was used successfully to design LNAs in the PCS Cellular handset receive band (1930-1990 MHz) with a noise figure less than 1 dB and input return loss of 14 dB or greater (1.5 VSWR). ■

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Author information

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